Transparent V-I protection in Audio Power Amplifers

(Part 1)

The desirability or lack thereof, of over-voltage and over-current protection for power semiconductors in audio power amplifiers remains a point of contention in the field. Michael Kiwanuka explans.

For example, Nelson Pass[2] appears to recommend multiple-transistor complementary output stages, as mandated by class-A operation, to circumvent the need for V-I protection of bipolar devices, while Rod Elliot[3] suggests that V-I limiters can be dispensed with altogether by adopting e-MOSFETs.

These views appear to be rather more widely accepted than they should, and constitute a charter for near heroic unreliability in amplifiers so designed. The zener diode-clamping of gate-source voltage for e-MOSFET's is thought by some[4,5] to be all that is required with regard to protection. While the zener diodes are mandatory, (ideally with $10V<V_{zener}<20V$ to prevent premature clamping), they only serve to protect the e-MOSFET gate oxide insulation from over-voltage destruction[6], and do nothing whatever to protect the device from accidental short circuits and forbidden voltage-current combinations that may occur when the amplifier is called upon to drive reactive loads.

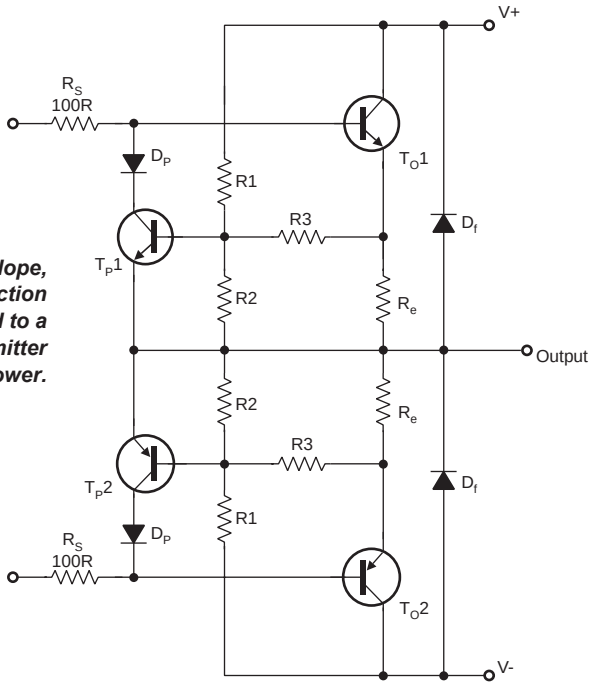


Figure 1: Single slope, linear foldback protection circuit applied to a complementary emitter follower.

The positive temperature coefficient of on-resistance[7], (and therefore negative temperature coefficient of drain current), enjoyed by e-MOSFETs eliminates the secondary breakdown phenomenon which is the bane of bipolar transistors, but does not constitute a licence for wilful violation of power dissipation limits in linear, audio-frequency applications. This is in contrast to ultrasonic switching usage, where e-MOSFET dissipation bounds can be blissfully ignored, and adherence to drain current and drain-source voltage limits will suffice.

All output stage semiconductors used in complementary, or quasi-complementary, (full or half bridge), linear audio power amplifiers, without exception, require V-I protection for reliable operation. However, such circuitry must be carefully designed to prevent premature activation during normal amplifier operation.

Single-slope, linear-foldback limiting

Many low to medium-power, (sub-100W), commercial audio amplifiers incorporate a single slope, linear foldback, voltage-current protection circuit, (figure 1), attributed to S.G.S. Fairchild Ltd. by Dr A.R. Bailey[8]. In practice the complimentary output transistors, T_{o1} and T_{o2}, may each consist of a compound arrangement of at least two transistors in series. The collector-emitter voltage, Vce, across T_{o1} is sensed by R_1, and R_3, while the output current, in the guise of a voltage developed across emitter resistor Re, is simultaneously monitored by R_3, and R_2. The voltages are thus summed algebraically at the base of the protection transistor, T_{p1}, which is driven into conduction, shunting voltage drive to T_{o1}, in the event of an over-voltage, over-current or simultaneous occurrence of both conditions in the output device.

The series resistor, Rs, (typically 100R), expedites this process by limiting the current required by T_{p1} to shunt voltage drive to T_{o1}. The freewheeling diode, D_F, protects the output device from excessive base-emitter reverse bias[9], due to over-rail voltage spikes generated by inductive loads, while D_F performs the same function for the small-signal protection transistor, by preventing its base-collector junction from being forward biased[10].

If the output approaches the negative supply rail while driving a sufficiently low impedance, the current sunk by T_{o2} generates an appreciable voltage drop across its emitter resistor. The output is therefore at a significantly higher potential than the common input to the complementary output stage. Transistor T_{o1} is reverse biased, and T_{p1}'s base-collector junction, in the absence of D_F, would be forward biased, resulting in current flow from emitter to collector.

Diode D_F prevents this form of spurious, inverse-active mode limiter activation by decoupling T_{p1}'s collector as T_{o1}'s base-emitter is reverse biased. The potential at T_{o1}'s emitter is then equal to the output voltage since, contrary to Duncan[11], T_{o1} is non-conducting and no current, except

negligible leakage, flows through its emitter resistor. By symmetry, the explanation above also applies to the negative half of the circuit.

A small-value capacitor is sometimes connected across the base-collector junction of each protection transistor[1], with a view to eliminating benign parasitic oscillation[12] that may occur sporadically in the network during the limiting process. These capacitors appear in parallel at A.C, and are entirely unsatisfactory, as they create an ill-defined and therefore undesirable feed-forward path around the output stage, shunting it out of the global feedback loop at high audio frequencies, precisely where the amplifier is most vulnerable with respect to non-linearity. Such vulnerability is due to a necessarily diminished feedback factor at high audio frequencies in the interest of Nyquist stability. Connecting the capacitor, (of the order of 1*n*0), across the base-emitter junction of each protection transistor is the preferred solution.

The resistor values for the arrangement in **Figure 1** are obtained by drawing the desired protection locus onto a linear scale graph of the output transistor's safe operating area, (S.O.A). One of the three resistors (usually R_3), is assigned an arbitrary value (typically 100R□R_3□1k), and the two remaining resistors calculated from simultaneous equations developed from two convenient points on the protection locus.

This arrangement requires that the linear protection locus intersects the S.O.A's Vce axis at a value greater than the sum of the moduli of the amplifiers voltage supplies, otherwise T_{p1} turns on under normal loading when the output swings negative, even with the output open-circuit. Similarly T_{p2} would be activated under normal output loading when the output swings positive. This effectively short-circuits the small signal circuit preceding the output stage directly to the output, causing gross and very audible distortion. Failure to adhere to the above condition appears to have caused some designers to erroneously abandon electronic S.O.A protection of any form altogether[1,13].

This requirement however, constitutes a significant limitation with regard to efficient utilisation of the comparatively large S.O.A in the low-Vce region of the graph, especially at high supply-rail voltages where, in the case of bipolar transistors, secondary-breakdown severely curtails flexibility in optimal placement of the protection locus. This is graphically illustrated in figure 2, for an amplifier with ±40V supply rails, using Motorola's excellent[14] 200W, MJL3281A-MJL1302A complementary power transistors.

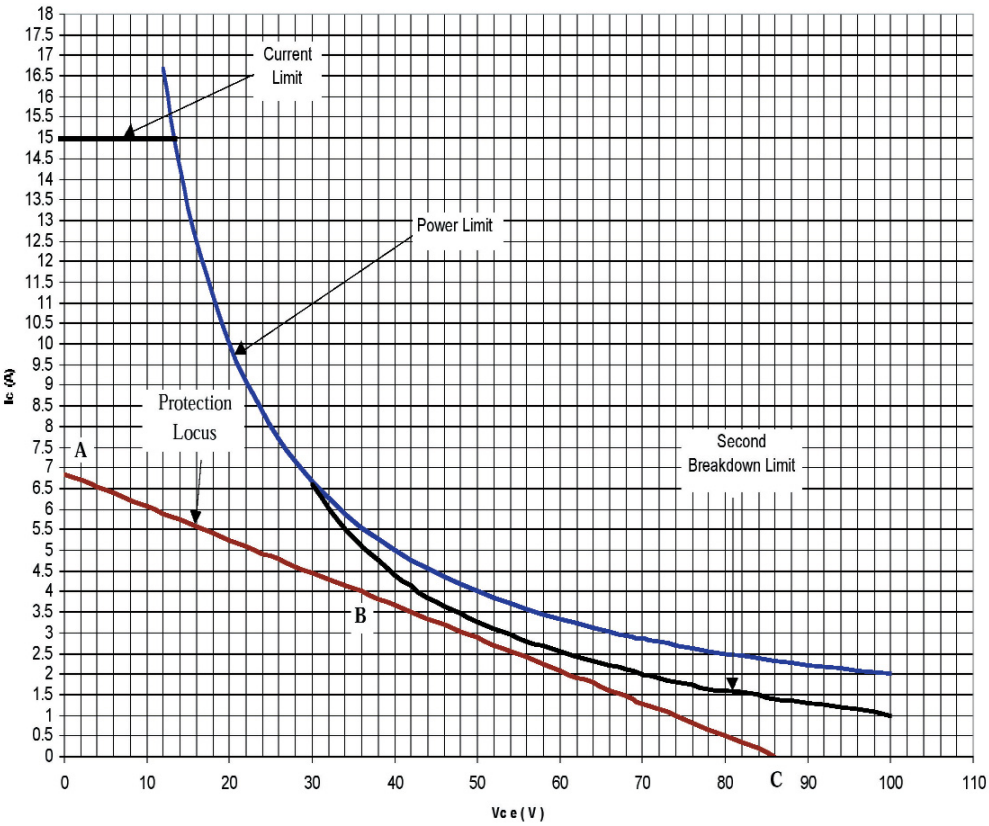


Figure 2: MJL3281A safe operating area with single slope, linear foldback protection locus

Only the positive half, **Fig. 3.**, of the circuit in figure 1 needs be used to calculate the required component values. Ideal devices are assumed, with infinite input impedance, zero saturation voltage, and zero ohmic resistance, the error thus accrued is negligible. Let V_{be}=0V6, R_3=220R, Re=0R22. Taking two arbitrary points, A and B on the locus, such that,

$$0.6 = \left\{0 \le V_{ce} < \left(2|V_{cc}| = 80V\right)\right\}$$

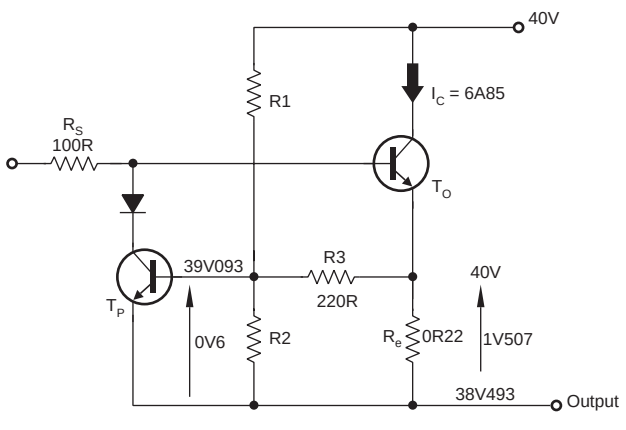


Figure 3: Output conditions at point A on the protection locus in figure 2.

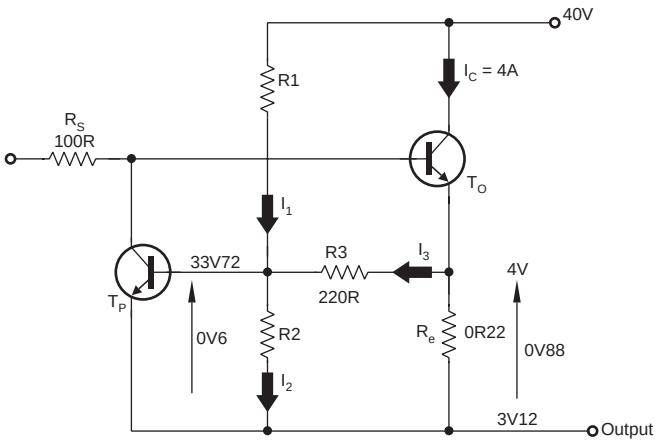


Figure 4: Output conditions at point B on the protection locus in

where for point A, Ic=6.85A; Vce=0V, and for point B, Ic=4A; Vce=36V, it follows from figure 3:

$$\frac{1.507R_2}{R_2 + R_1 220/(R_1 + 220)} \quad (1)$$

With reference to figure 4:

$$I_2 = I_1 + I_3 \quad (2)$$

$$0.6/R_2 = (40 - 3.72)/R_1 + (4 - 3.72)/R_3$$

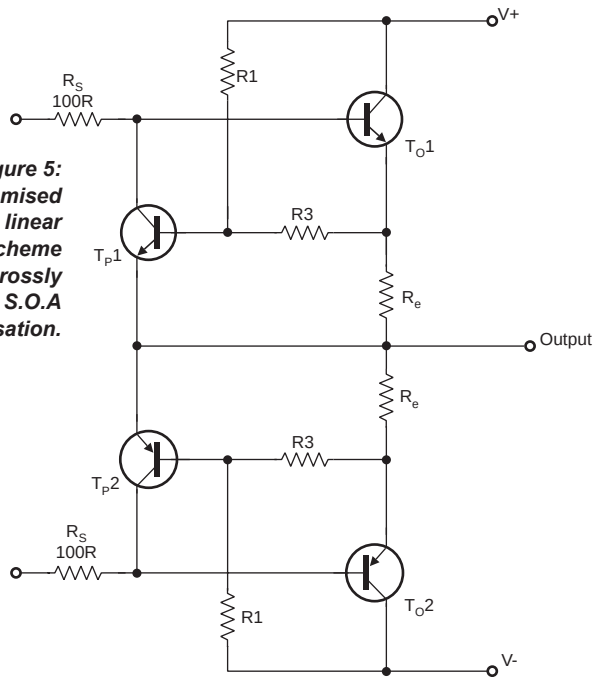


Figure 5: Compromised single slope, linear foldback scheme resulting in grossly inefficient S.O.A utilisation.

$$0.6 = R_2(36.28/R_1 + 0.28/220) \quad (3)$$

Solving (1) and (3) simultaneously gives R_1≈12K4 and R_2≈ 143R0. To afford an acceptable degree of precision, it is recommended where necessary, that these values be made up from series, or parallel combinations of 1% resistors.

When the output swings to –40V, then 80V appears across R_3 in series with R_2//R_3, to a good first approximation. Therefore the voltage present at the base of the protection transistor, T_p, is given by:

$$V_{be} \approx \frac{80(R_2 // R_3)}{(R_2 // R_3) + R_1} \approx 0V55$$

It follows therefore that subject to instantaneous collector current, i_c, being less than the maximum permissible collector current, $I_{C(MAX)}$, at V_{ce}≥2|V_{cc}|, spurious activation of T_p cannot occur. A general expression which allows the rapid verification of the compliance of any amplifier using single slope, linear foldback limiting may developed:

$$\left|\frac{2V_{cc}(R_2 // R_3)}{\{(R_2 // R_3) + R_1\}}\right| < 0V6$$

$$\left|\frac{2V_{cc}R_2R_3}{(R_2R_3 + R_1R_2 + R_1R_3)}\right| < 0V6 \quad (4)$$

Equation 4 is valid subject to the following condition:

$$i_C < I_{C(MAX)}|_{V_{ce} \approx 2|V_{cc}|} \quad (5)$$

This condition is invariably fulfilled during normal operation, as no practical loudspeaker system would demand that the output transistor sustain V_{ce}≥2|V_{cc}|, while providing any appreciable current.

Figure 5 shows a common variation[11,14,15], on the

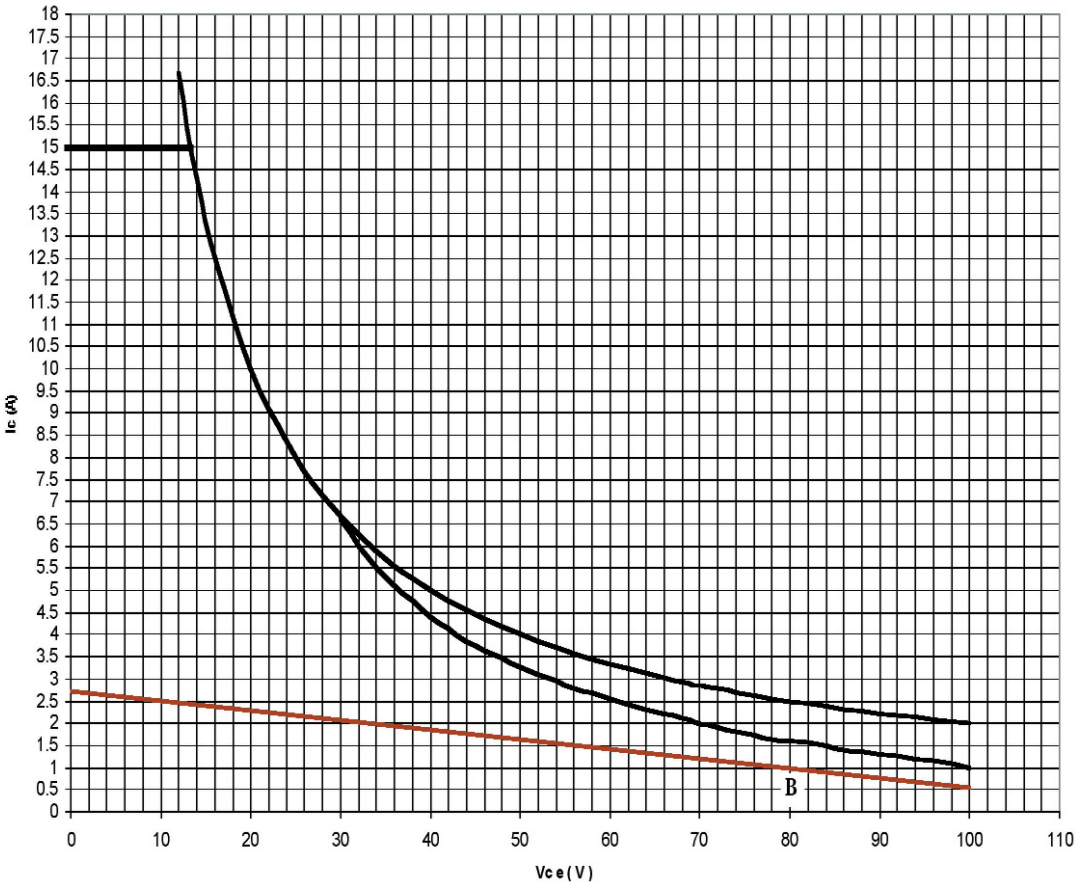


Figure 6: Linear protection locus clearly shows inflexibility of scheme in figure 5.

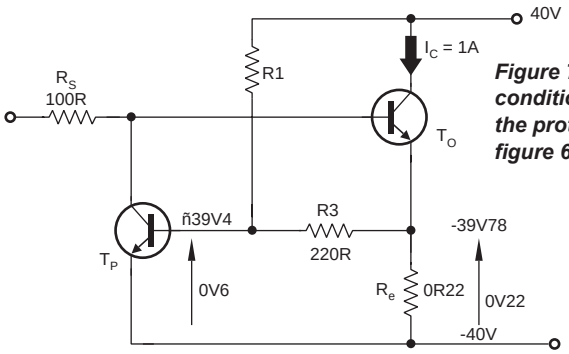


Figure 7: Output conditions at point B on the protection locus in figure 6.

single slope, linear foldback limiter of figure 1, with resistor R_2 excised, so that from equation 4:

$$\left|\frac{2V_{cc}R_3}{\left\{R_3+R_1+\left(R_1\frac{R_3}{R_2}\right)\right\}}\right|<0V6$$

Since $R_2 \rightarrow \infty$, then:

$$\left|\frac{2V_{cc}R_3}{(R_3+R_1)}\right|<0V6$$

The optimal protection locus for this network **Fig. 6.**, is plotted so that calculated resistor values comply with the above condition. This scheme is atrociously inefficient, as for a nominal V_{ce}²0V and R_e=0R22, resistors R_1 and R_3 are in parallel, and collector current, I_c, is perforce prematurely limited to,

$$\left\{I_c\big|_{V_{ce}\approx 0V}<\left(V_{be}/R_e\approx 2A7\right)\right\}$$

A value of R_e=0R1 gives a modest improvement, with,

$$\left\{I_c\big|_{V_{ce}\approx 0V}<\left(V_{be}/R_e\approx 6A0\right)\right\}$$

The protection locus is realised by deriving output stage conditions **Fig. 7.** for a single, arbitrary point, B on the locus, subject to, $\{0<V_{ce}<2|V_{cc}|\}$. With V_{cc}=40V, R_e=0R22, R_3=220R and noting that R_1, R_3 constitute a simple voltage divider:

$$R_1\approx\frac{(40+39.4)}{(-39.4+39.78)/220R}\approx 46K$$

This unwarranted dependence on the value of R_e is unacceptable, as in some applications such as output stages comprised of paralleled, complementary e-MOSFET pairs, ($0R1<R_e\square 1R0$), may be required to ensure equable current sharing.

Driving reactive loads.

A clear appreciation of the nature of the amplifierís load is required to establish the bounds within which the V-I limiter must remain inactive. **Figure 8** shows an ideal complementary emitter follower, (in Electronics Workbench's excellent Multisim professional simulator[16]), used to drive a standard (8ohms 0°) test load to ±40V supply rails.

The plots obtained in **Fig. 9.** show that the voltage v_{ce}, across T_{o1} is precisely 180° out of phase with the current, i_c,, its required to source; the voltage across the device is a minimum when its collector current is at a maximum, and vice versa. Instantaneous power dissipation is merely the product of instantaneous device voltage and current. Peak transistor dissipation, $P_{d(max)}$²50W, occurs twice in T_{o1}'s conducting half-cycle, at half the peak load voltage, (V_{out}/2²V_{cc}/2) and half the peak load current, $i_{c(peak)}$/2.

As the (8ohms 0°) load line lies well below the linear protection locus in figure 10, (reproduced from figure 2),

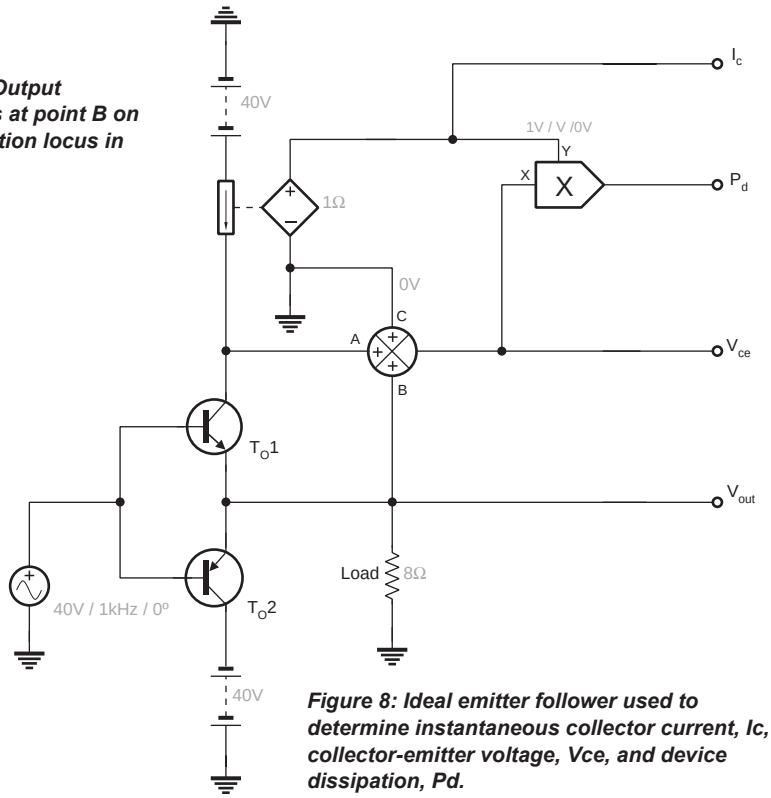


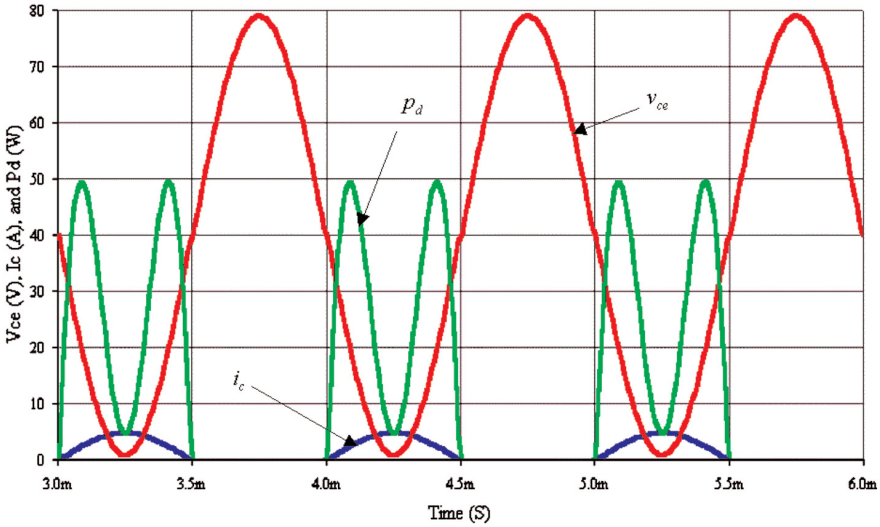
Figure 8: Ideal emitter follower used to determine instantaneous collector current, Ic, collector-emitter voltage, Vce, and device dissipation, Pd.

it is clear that a single pair of MJL3281A-MJL1302A power transistors, operating from ±40V rails will comfortably drive an 8ohms dummy load to clipping without V-I limiting. This however, will certainly not be the case with loudspeaker loads, which are invariably reactive[17,18]. An amplifier with 'high-fidelity' aspirations, intended to drive full-range, multiple-transducer loudspeaker systems, including electrostatics, should at least be capable of driving a (4ohms ±60°) impedance without V-I limiting.

A (4ohms –60°) impedance was devised by driving a 2ohms0 resistor in series with a 45µ 9441 capacitor at 1Khz with the ideal complementary emitter follower in figure 8. The traces thus obtained, **Fig. 11.**, were used to plot the (4ohms ±60°) load line in figure 10. Peak transistor dissipation, $P_{d(max)}$²352.9W, occurs at v_{ce}²45.97V, and i_c²7.68A.

In other words **Fig 12.**, because current leads voltage in a capacitive impedance, the NPN transistor, T_{o1} in figure 8, is required to source ²7.68A when the output swings

Figure 9: Instantaneous Vce, Ic, and Pd in sourcing output transistor, driving 100W into (*8*ohms 6*0*°).



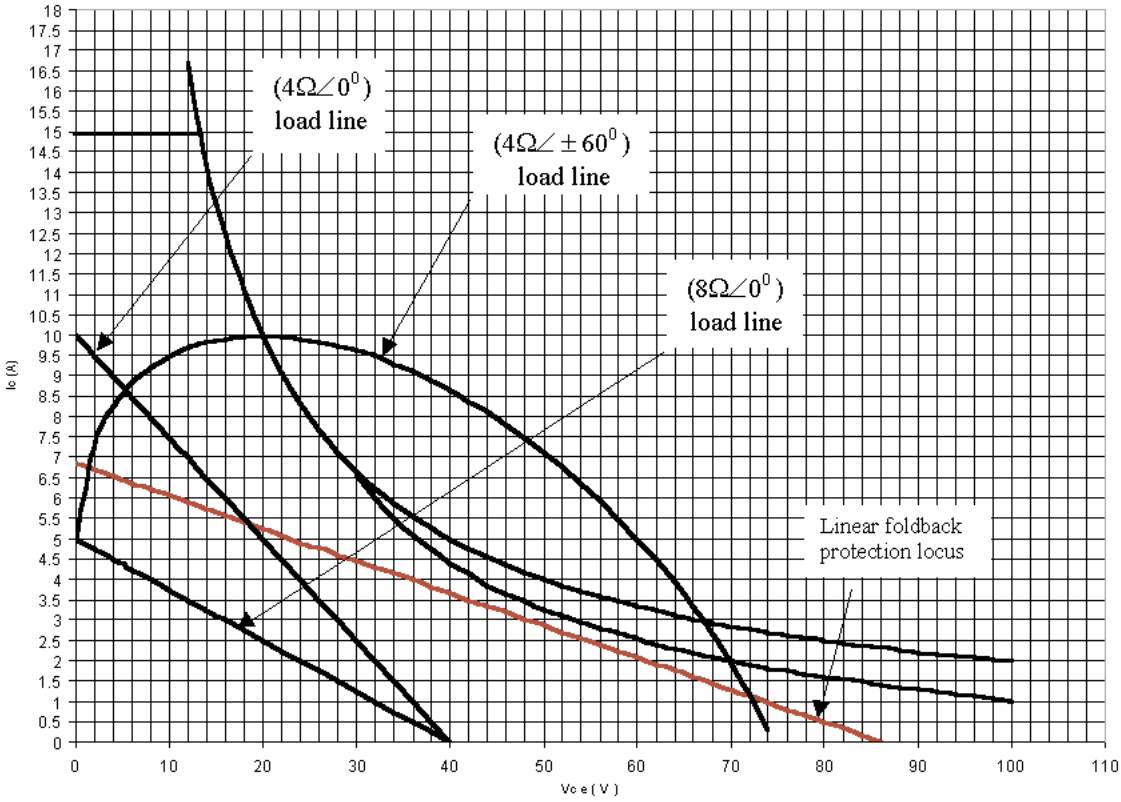


Figure 10: Reactive load gives rise to an elliptical line, resulting in more than seven times greater peak device dissipation than for the (8ohms 60°)

away from the negative supply rail to ²–5.97V. Similarly, the PNP device, T_{o2}, must sink ²7.68A when the output swings to +5.97V from +Vcc. Note that the crossover discontinuity in the output voltage characteristic (figure 12), now precedes zero crossing by 60°, at $|V_{out}|$²35V.

For a (4ohms +60°) inductive impedance, in which current lags voltage, the output conditions are reversed, with the load demanding 7.68A from T_{o1} when the output swings from the positive supply to –5.97V. Regardless of the nature of the load however, device voltage, v_{ce}, and load voltage, v_{out}, are always 180° out of phase, and being a voltage follower, the input voltage is always in phase with v_{out}.

The linear foldback protection locus of figure 10 only permits 3.1A at Vce=45.97V, therefore a minimum of three, (ideally four), output pairs are required to drive a notional (4ohms ±60°) loudspeaker system from ±40V supply rails without intrusive limiter activation. On this basis and using other established techniques[12,19], including D.C. offset, and thermal overload protection, a reliable, low distortion, 100W into (4ohms ±60°) class-B amplifier may be constructed.

As the cost of power transistors is significant, there is a compelling financial incentive to minimise the number of devices used by utilising the S.O.A as efficiently as possible. To this end it has been suggested[11] that ideally the protection locus should closely match the bounds of the S.O.A. This is unnecessary, as reactive load drive primarily requires that current delivery in the $|V_{cc}| \square V_{ce} < 2|V_{cc}|$ region be maximised without violating D.C safe operating limits. In general an optimally located, non-linear protection locus with no more than one breakpoint should suffice.

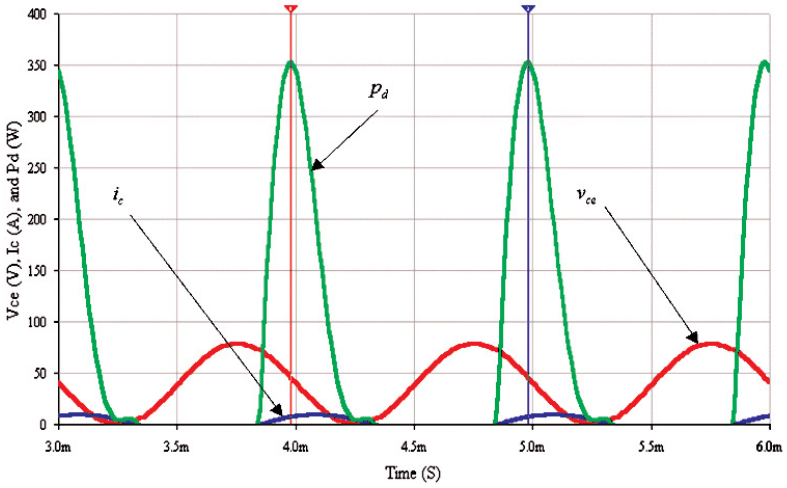


Figure 11: Instantaneous Vce, Ic, and Pd in sourcing output transistor, driving 150W into 4ohms 60°).

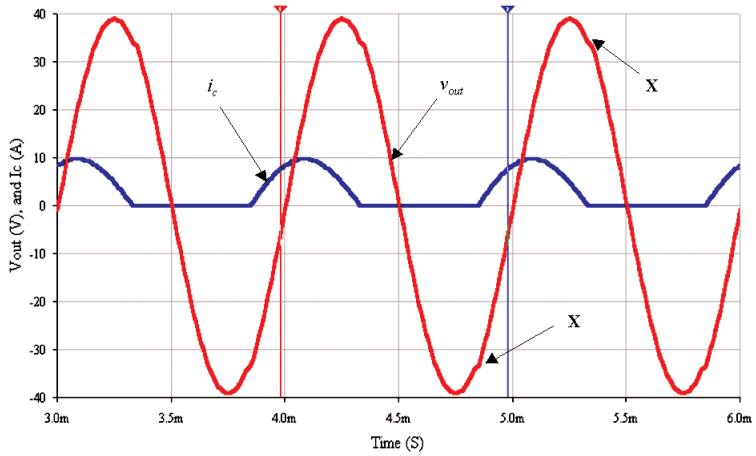


Figure 12: Transistor T_{o2} delivers 7.68A to the (4ohms 60°) load when output swings away from -Vcc to -5.97V. Note that the crossover discontinuity marked X precedes zero voltage crossing by 60°.

Single slope, single breakpoint non-linear foldback limiting.

Introducing a zero-gradient segment **Fig. 13**, at some optimal point in the protection locus permits the enhancement of current delivery at the low-Vce end of the S.O.A., without significantly compromising available current at higher device voltages. The single slope, linear foldback 'protocol', (equation 4), is made redundant, as the protection locus does not cross the Vce-axis at any point. This scheme is briefly mentioned in reference [20],